

## MOS FIELD EFFECT TRANSISTOR $\mu$ PA1724

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

### \* DESCRIPTION

The  $\mu$ PA1724 is N-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and so on.

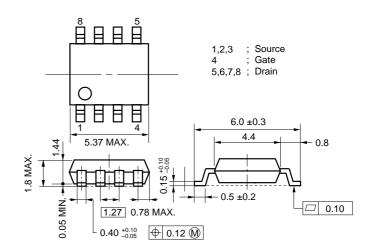
### **FEATURES**

- 2.5-V gate drive and low on-resistance
  - RDS(on)1 = 11.0 m $\Omega$  MAX. (VGS = 4.5 V, ID = 5.0 A)
- ★ RDS(on)2 = 12.0 m $\Omega$  MAX. (VGS = 4.0 V, ID = 5.0 A)
  - $R_{DS(on)3} = 15.0 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = 2.5 \text{ V, ID} = 5.0 \text{ A)}$
  - Low Ciss: Ciss = 1850 pF TYP.
  - Built-in G-S protection diode
  - Small and surface mount package (Power SOP8)

### **ORDERING INFORMATION**

PART NUMBER	PACKAGE		
μPA1724G	Power SOP8		

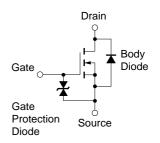
### PACKAGE DRAWING (Unit: mm)



### ABSOLUTE MAXIMUM RATINGS (TA = 25°C, All terminals are connected.)

Drain to Source Voltage (Vgs = 0 V)	VDSS	20	V
Gate to Source Voltage (Vps = 0 V)	Vgss	±12	V
Drain Current (DC)	ID(DC)	±10	Α
Drain Current (pulse) Note1	D(pulse)	±40	Α
Total Power Dissipation $(T_A = 25^{\circ}C)^{Note2}$	Рт	2.0	W
Channel Temperature	Tch	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C

### **EQUIVALENT CIRCUIT**



- **Notes 1.** PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1 %
  - 2. Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 2.2 mm

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.



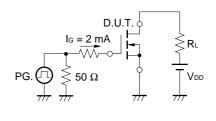
### ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)

	CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
	Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	Vgs = 4.5 V, lb = 5.0 A		8.6	11.0	mΩ
*		R <sub>DS(on)2</sub>	Vgs = 4.0 V, Ip = 5.0 A		8.8	12.0	mΩ
		R <sub>DS(on)3</sub>	V <sub>G</sub> S = 2.5 V, I <sub>D</sub> = 5.0 A		11.0	15.0	mΩ
	Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	0.5	0.84	1.5	V
	Forward Transfer Admittance	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.0 A	10.0	19		S
	Drain Leakage Current	Ipss	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			10	μΑ
	Gate to Source Leakage Current	Igss	Vgs = ±12 V, Vps = 0 V			±10	μΑ
	Input Capacitance	Ciss	V <sub>DS</sub> = 10 V		1850		pF
	Output Capacitance	Coss	V <sub>G</sub> S = 0 V		610		pF
	Reverse Transfer Capacitance	Crss	f = 1 MHz		320		pF
	Turn-on Delay Time	td(on)	ID = 5.0 A		43		ns
	Rise Time	tr	V <sub>GS(on)</sub> = 4.5 V		170		ns
	Turn-off Delay Time	td(off)	V <sub>DD</sub> = 10 V		90		ns
	Fall Time	tf	R <sub>G</sub> = 10 Ω		130		ns
	Total Gate Charge	Q <sub>G</sub>	ID = 10 A		18		nC
t	Gate to Source Charge	Qgs	V <sub>DD</sub> = 16 V		3.2		nC
t	Gate to Drain Charge	Q <sub>GD</sub>	Vgs = 4.5 V		7.8		nC
	Body Diode Forward Voltage	V <sub>F</sub> (S-D)	IF = 10 A, VGS = 0 V		0.78		V
	Reverse Recovery Time	trr	IF = 10 A, VGS = 0 V		45		ns
	Reverse Recovery Charge	Qrr	di/dt = 100 A / μs		40		nC

### **TEST CIRCUIT 1 SWITCHING TIME**

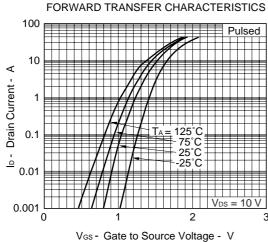
# PG. $\bigcap_{RG} RG = 10 \Omega$ $V_{GS} \bigvee_{Wave Form} 0 0 0 0 \%$ $V_{GS} \bigvee_{Wave Form} 0 0 0 0 \%$

### TEST CIRCUIT 2 GATE CHARGE

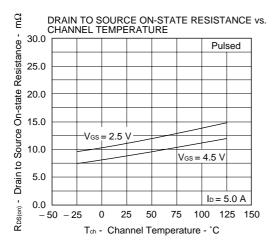


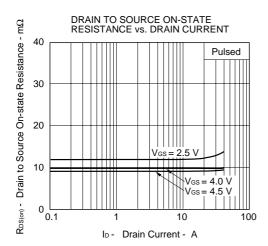


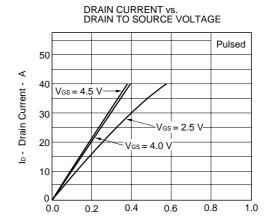
### TYPICAL CHARACTERISTICS (TA = 25 °C)

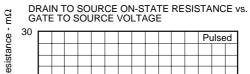




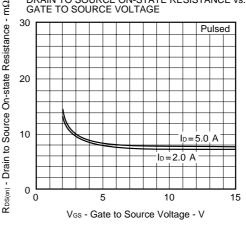


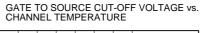


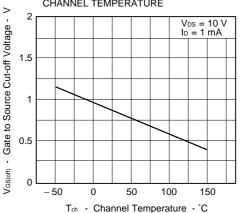




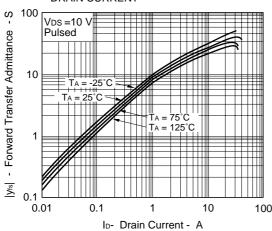
V<sub>DS</sub> - Drain to Source Voltage - V

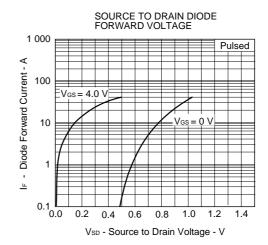


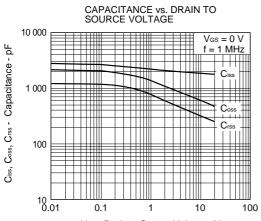


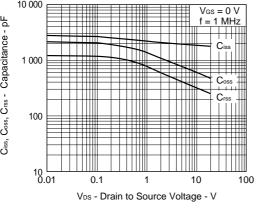


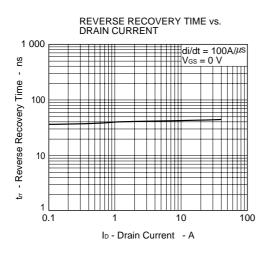
### FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

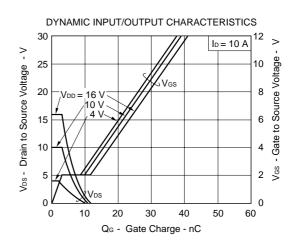


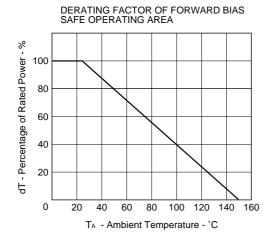


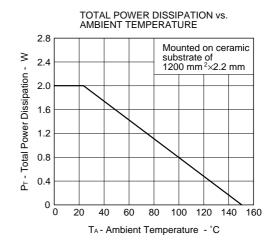


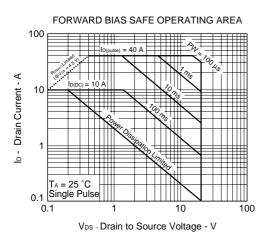




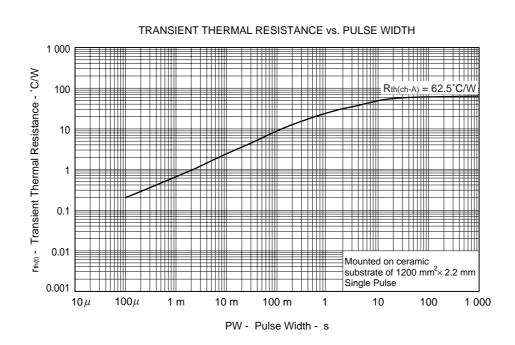








**Remark**Mounted on ceramic substrate of 1200 mm<sup>2</sup> x 2.2 mm



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NEC

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NEC  $\mu$ PA1724

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